REMARKS

The claims are claims 1 to 4, 9, 10, 14, 15, 17 and 18.

Claims 1, 2, 3, 14 and 15 have been amended. Claims 5 to 8, 11 to 13 and 16 are canceled. New claims 17 and 18 are added. Claims 1, 2, 3, 14 and 15 are amended to distinguish over the references. Claims 17 and 18 correspond to respective claims 2 and 3 in apparatus form dependent upon apparatus independent claim 14.

Claims 1 to 3, 9 and 14 were rejected under 35 U.S.C. 102(e) as anticipated by Bausch U.S. Patent No. 6.339,816.

Claims 1 and 14 recite subject matter not anticipated by Bausch. Claim 1 recites "invalidating a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the shared indicator in response to an invalidate TLB entry command issued from the processor and not changing data in any other memory." Claim 14 recites "control circuitry connected to the storage circuitry, wherein the control circuitry is responsive to an invalidate TLB entry command to invalidate entries within said storage circuitry qualified by the shared indicator field not change data in any other memory." These recitations differ from the disclosure of Bausch in several aspects. First, claims 1 and 14 recite "an invalidate TLB entry command." Bausch fails to disclose such a command. Bausch teaches his invalidation of table lookaside buffer entries is in response to a write attempted to a write-protected portion of memory. Bausch states at the Abstract, lines 1 to 5:

> "When there are write accesses to user pages in a data processing system that are marked as write-protected in a translation memory, the method checks, after an interrupt request, a corresponding page table entry and also whether there is an access with system authorization."

Bausch states at column 1, lines 41 to 46:

PAGE 9/14 * RCVD AT 1/27/2004 10:38:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:972 917 4417 * DURATION (mm-ss):05-04

"This is achieved by the present invention in that the internal control is additionally permitted to write on write-protected user pages as well. In this way stored data can be corrected, or new program code that is shared by several tasks can be written from the system side."

Bausch states at column 2, lines 21 to 31:

"According to an embodiment of the present inventive method, there is a write access present, as shown in step 1 of the sole FIGURE, according to step 2 it is checked whether the control bit D that marks the write protection is set (i.e., equal to "1"). If it is, then the access can be permitted according to step 3. If not, then an interrupt request TLB MOD.EXC is triggered according to step 4. The processing of this interrupt request leads in known fashion to the checking of the appertaining page table entry according to step 5. If there is not a true violation of the write protection, then the access can be allowed."

Thus Bausch teaches invalidation of some entries in the table lookaside buffer responsive to a write operation to a write-protected portion of memory. This does not anticipate the "invalidate TLB entry command" recited in claims 1 and 14. Accordingly, claims 1 and 14 are allowable over Bausch.

Second, claims 1 and 14 each recite the table lookaside operation does not change "data in any other memory." This is directly contrary to the teaching of Bausch, which discloses invalidation of table lookaside buffer entries in response to a permitted write to write-protected memory. Thus Bausch clearly does change other memory. Accordingly, claims 1 and 14 are allowable over Bausch.

Third, claims 1 and 14 each recite operations responsive to "an invalidate TLB entry command." Bausch teaches another event triggers the invalidation operation. Bausch states at column 1, line 60 to column 2, line 2:

PAGE 10/14 * RCVD AT 1/27/2004 10:38:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:972 917 4417 * DURATION (mm-ss):05-04

"The write authorization for the system is dropped when the operating mode is changed from the system to the user, respectively, in that it is first checked whether one of the control bits that forms the indicators is set. Given a set control bit for a globally used page, then all address entries in the translator memory that are related to globally used pages and whose control bit for the write authorization is set are declared invalid. On the other hand, given a set bit for a page that is used task-locally, all entries for the related task are declared invalid. This can be accomplished easily by changing the appertaining address space identifier ASID."

Bausch further states at column 2, lines 65 to 67:

"For this purpose, the present invention uses the two control bits GL and TL that are checked after the operating mode has been changed."

Thus Bausch clearly teaches the event triggering the table lookaside invalidation is a change in the operating mode and not the "invalidate TLB entry command" recited in claims 1 and 14. Accordingly, claims 1 and 14 are allowable over Bausch.

Claims 2 and 3 recite subject matter not anticipated by Bausch. Claim 2 recites invalidating "in response to an invalidate shared TLB entry command comprises invalidating a translated memory address in the TLB only if the corresponding shared indicator indicates the translated memory address is shared by more than one of the plurality of program tasks." Claim 3 recites invalidating "in response to an invalidate task TLB except shared command comprises invalidating a translated memory address in the TLB only if the corresponding task identification value indicates the program task identified by said invalidate task TLB entry except shared command and the corresponding shared indicator indicates the translated memory address is not shared by more than one of the plurality of program tasks. These claims clearly recite that the table lookaside buffer entries invalidated are selected by the type

PAGE 11/14 * RCVD AT 1/27/2004 10:38:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:972 917 4417 * DURATION (mm-ss):05-04

of command and by the data in the table lookaside buffer. The FINAL REJECTION cites Bausch column 3, lines 1 to 5 as anticipating the subject matter in claims 2 and 3. This portion of Bausch states:

> "If the control bit GL is set, then all entries in the translation memory TLB whose control bit D is set and that relate to global user pages must be declared invalid.
> "Alternatively if the control bit TL is set, then only the entries of the corresponding task must be declared invalid."

This portion of Bausch occurs immediately following column 2, lines 65 to 67 quoted above. Accordingly, Bausch fails to teach different action taken based upon different received commands as recited in claims 2 and 3. Instead, Bausch teaches alternative actions based upon data within the table lookaside buffer in response to the same event of changing the operating mode. In the absence of teaching of separate actions in response to different commands, claims 2 and 3 are allowable over Bausch.

Claim 9 recites subject matter not anticipated by Bausch. Claim 9 recites "including within the set of page translation tables the shared indicator for each translated memory address." Bausch fails to teach which if any access control bits are stored in the page table entry. The MIPS R4000 User's Manual likewise fails to teach which access control bits if any are stored in the page table entry. Accordingly, these references fail to teach storage of the shared indicator in the page translation table as recited in claim 9.

Claims 4 and 15 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Bausch and Slater, "A Guide to RISC Microprocessors."

Claims 4 and 15 recite subject matter not made obvious by the combination of Bausch and Slater. Claim 4 recites "the TLB has

PAGE 12/14 * RCVD AT 1/27/2004 10:38:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729308 * CSID:972 917 4417 * DURATION (mm-ss):05-04

several levels, and wherein the step of invalidating encompasses all of the several levels of the TLB." Claim 15 recites a second level storage circuitry and that the control circuitry is "responsive to an invalidate TLB entry command to invalidate selected ones of the plurality of entry locations in the second storage circuitry qualified by the shared indicator field." Slater teaches that the table lookaside buffer of Bausch could include multiple levels. However, Bausch fails to make obvious invalidating the table lookaside buffer at plural levels. The Applicant respectfully submits that the teaching of Bausch would motivate one skilled in the art away from this subject matter. Bausch teaches changing the dirty bit D, which indicates write protection, only within the table lookaside buffer and not within the page table entry (see column 2, lines 50 to 53). The invalidation taught in Bausch on entering the user operating mode forces a table lookaside buffer miss on the next access to the corresponding memory addresses. This requires the reloading of the table lookaside buffer from the page table entry. Changing the D bit in other levels of translation tables would prevent return to the proper state for the user operating mode. Accordingly, it would not be obvious from Bausch and Slater to invalidate plural levels. Accordingly, claims 4 and 15 are allowable over the combination of Bausch and Slater.

Claim 10 was rejected under 35 U.S.C. 103(a) as anticipated by Bausch.

Claim 10 recites subject matter not anticipated by Bausch. Claim 10 recites "maintaining a set of page translation tables for providing each translated memory address, wherein the shared indicator for each translated memory address is not included within the set of page translation tables." The FINAL REJECTION states at page 6, lines 4 to 8:

PAGE 13/14 * RCVD AT 1/27/2004 10:38:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:972 917 4417 * DURATION (mm-ss):05-04

"As per claim 10, Bausch does not teach not storing the control bit GL in the page translation tables. However it would have been obvious to one of ordinary skill in the art to have not included the control bit GL in the page translation tables because the status of a particular entry as being related to multiple tasks may change dynamically, and not storing information that may change quickly within the page tables would save memory, thereby reducing system cost."

This in fact is the opposite argument the Examiner directed to claim 9 that inclusion within the page translation table would be obvious. The Applicant respectfully submits that Bausch includes no teaching regarding this claimed feature. Accordingly, the Examiner's argument is not based upon any teaching of Bausch. Accordingly, claim 10 is allowable over Bausch.

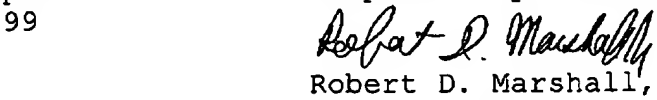
Claims 17 and 18 recite subject matter of the same scope as claims 2 and 3 except in apparatus form. Accordingly, claims 17 and 18 are likewise allowable.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,



Robert D. Marshall, Jr.
Reg. No. 28,527

PAGE 14/14 * RCVD AT 1/27/2004 10:38:20 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:972 917 4417 * DURATION (mm-ss):05-04